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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/592,572	06/12/2000	Richard Dellacona	QUAD:55767	4159

7590 05/09/2006

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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 05/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/592,572	DELLACONA, RICHARD	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-13,16-21,23-31 and 34-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-13,16-21,23-31 and 34-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' Response mailed on April 6, 2006. Claims 1-3, 5-13, 16-21, 23-31 and 34-36 of the application are pending. This office action is made final.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-3, 5, 7 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Leshem** (U.S. Patent 5,729,763) in view of **Espy** (International Application WO 98/21660), and further in view of **Horst et al.** (U.S. Patent 6,496,940), **Hillis** (U.S. Patent 5,978,570), **Dekoning et al.** (U.S. Patent 6,055,228), **Swanson et al.** (U.S. Patent 6,580,531) and **Brant et al.** (U.S. Patent 5,548,711).

4.1 **Leshem** teaches Data storage system. Specifically, as per Claim 1, **Leshem** teaches a high speed mass storage system (CL1, L4-8; CL1, L33-37; Abstract, L11-14).

Leshem does not expressly teach a high speed mass storage system which is readily expandable to increase its storage capacity while the system is in operation; and first and second mass storage modules. **Espy** teaches a high speed mass storage system which is readily expandable to increase its storage capacity while the system is in operation (Page 1, L19-24); and first and second mass storage modules (Fig. 1, Items 10 and 110; Page 1, L19-24). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Leshem** with the system of **Espy** that included high speed mass storage system which would be readily expandable to increase its storage capacity while the system was in operation; and first and second mass storage modules because that would enable to add an additional disk array chassis to the existing system when additional memory space was required, without shutting down the existing system (Page 1, L19-24).

Leshem and **Espy** do not expressly teach a first server including a first controller and at least one CPU; and a second server including a second controller and at least one CPU. **Horst et**

al. teaches a first server including a first controller and at least one CPU; and a second server including a second controller and at least one CPU (Fig. 1A, Items 12A and 14A; Items 12B and 14B; Abstract, L1-8). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Leshem** and **Espy** with the system of **Horst et al.** that included a first server including a first controller and at least one CPU; and a second server including a second controller and at least one CPU because that would provide a fault tolerant architecture and hardware redundancy (CL4, L38-41).

Leshem and **Horst et al.** do not expressly teach each mass storage module including a plurality of plug-in storage devices for storing information. **Espy** teaches each mass storage module including a plurality of plug-in storage devices for storing information (Fig. 1, Items 12 of Items 10 and 110; Page 5, L16-17). One of ordinary skill in the art at the time of Applicants' invention would know the motivation to modify the system of **Leshem** and **Horst et al.** with the system of **Espy** that included each mass storage module including a plurality of plug-in storage devices for storing information because the storage capacity of the mass storage module would be increased proportional to the number of plug-in storage devices for storing information. See **Hillis** (CL11, L29-33).

Leshem and **Horst et al.** do not expressly teach each mass storage module including a storage device bypass circuit board associated with each storage device each storage device being plugged into a connector on the storage device bypass circuit board. **Espy** teaches each mass storage module including a storage device bypass circuit board associated with each storage device each storage device being plugged into a connector on the storage device bypass circuit board (Fig. 1, Item 26 of Items 10 and 110; Page 5, L26-27; Page 5, L30 to Page 6, L2).

One of ordinary skill in the art at the time of Applicants' invention would know the motivation to modify the system of **Leshem** and **Horst et al.** with the system of **Espy** that included each mass storage module including a storage device bypass circuit board associated with each storage device each storage device being plugged into a connector on the storage device bypass circuit board because that would enable connecting the storage device to the daisy-chain communication loop, when the device was enabled; and when failure or absence of a storage device was detected bypassing the storage device by connecting the daisy chain loop without the device. See **Dekoning et al.** (CL11, L52-60).

Leshem and **Horst et al.** do not expressly teach each mass storage module including a module bypass circuit board. **Espy** teaches each mass storage module including a module bypass circuit board (Page 2, L5-23; Fig. 1, Item 40; Page 6, L7-16).

Leshem, Espy and **Horst et al.** do not expressly teach the module bypass circuit board including an optical input/ output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals. **Swanson et al.** teaches the module bypass circuit board including an optical input/ output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals (Fig. 2; CL1, L19-42). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Leshem, Espy** and **Horst et al.** with the system of **Swanson et al.** that included the module bypass circuit board including an optical input/ output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals

because optical transmission would provide large capacity for digital transmission in computer/communication networks (CL1, L26-29).

Leshem, Horst et al. and **Swanson et al.** do not expressly teach that the optical input/output connectors of the first and second mass storage modules are connected by a fiber optic transmission medium such that signals are communicated between the first and second mass storage modules in the form of light. **Espy** teaches that the optical input/output connectors of the first and second mass storage modules are connected by a fiber optic transmission medium such that signals are communicated between the first and second mass storage modules in the form of light (Page 2, L29 to Page 3, L6; Page 6, L7-16). One of ordinary skill in the art at the time of Applicants' invention would know the motivation to modify the system of **Leshem, Horst et al.** and **Swanson et al.** with the system of **Espy** that included the optical input/output connectors of the first and second mass storage modules being connected by a fiber optic transmission medium such that signals were communicated between the first and second mass storage modules in the form of light because the fiber optic transmission would provide high data rates. See **Leshem** (CL1, L31-35).

In addition, **Hillis** teaches that the optical input/output connectors of the first and second mass storage modules are connected by a fiber optic transmission medium such that signals are communicated between the first and second mass storage modules in the form of light (Fig. 5; Fig. 6; CL10, L59 to CL11, L5; CL11, L29-33; CL11, L34-51). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Leshem, Horst et al.** and **Swanson et al.** with the system of **Hillis** that included the optical input/output connectors of the first and second mass storage modules being connected by a fiber

optic transmission medium such that signals were communicated between the first and second mass storage modules in the form of light because fiber optic communication lines would have high band width and data rates of 100 megabits per second (CL11, L43-48).

Leshem teaches controller providing a communication path between the first server and some of the storage devices through its associated storage device bypass circuit board (CL3, L33-36; CL3, L40-50). **Leshem, Espy** and **Swanson et al.** do not expressly teach the first controller providing a communication path between the first server and each storage device; and the second controller providing a communication path between the second server and each storage device. **Horst et al.** teaches the first controller providing a communication path between the first server and each storage device; and the second controller providing a communication path between the second server and each storage device (CL16, L6-15; Fig. 1, Items 14A and 14B). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Leshem, Espy** and **Swanson et al.** with the system of **Horst et al.** that included the first controller providing a communication path between the first server and each storage device; and the second controller providing a communication path between the second server and each storage device because that would allow each processing system to be operated in simplex mode in which the CPU's of the two systems operate in independent fashion (CL16, L6-9).

Leshem teaches the first controller providing a communication path between the first server and some of the storage devices through its associated storage device bypass circuit board (CL3, L33-36; CL3, L40-50). **Horst et al.** teaches the first controller providing a communication path between the first server and each storage device; and the second controller

providing a communication path between the second server and each storage device (CL16, L6-15; Fig. 1, Items 14A and 14B). **Leshem, Horst et al.** and **Swanson et al.** do not expressly teach the first controller providing a communication path between the first server and each storage device through its associated storage device bypass circuit board and through the module bypass circuit board, the second controller providing a communication path between the second server and each storage device through its associated storage device bypass circuit board and the module bypass circuit board. **Espy** teaches the controller providing a communication path between the server and each storage device through its associated storage device bypass circuit board and through the module bypass circuit board (Fig. 1, Item 16; Items 12, 22 and 26). One of ordinary skill in the art would know the motivation to combine the system of **Leshem, Horst et al.** and **Swanson et al.** with the system of **Espy** that included the controller providing a communication path between the server and each storage device through its associated storage device bypass circuit board and through the module bypass circuit board because that would enable connecting the storage device and the module bypass circuit board to the daisy-chain communication loop, when the device and additional module were enabled; and when failure or absence of a storage device or additional module was detected bypassing the storage device or the additional module by connecting the daisy chain loop without the device. See **Dekoning et al.** (CL11, L52-60).

Leshem, Espy, Horst et al. and **Swanson et al.** do not expressly teach at least one of the servers being operative to establish direct communication between the first and second controllers, and the first and second controllers being operative to maintain direct communication between the first and second controllers independent of the at least one CPU of

the first server and the at least one CPU of the second server. **Brant et al.** teaches at least one of the servers being operative to establish direct communication between the first and second controllers, and the first and second controllers being operative to maintain direct communication between the first and second controllers independent of the at least one CPU of the first server and the at least one CPU of the second server (CL7, L20-28; each controller includes a separately programmable processor which can act independently of the CPU to control storage units; Fig. 4; there are two controllers connected to the CPU; each controller has direct communication with the other controller; CL12, L64 to CL13, L8; Fig. 8; each controller communicates with the other controller using the controller processor and data link interface, independent of the CPU; CL18, L42-52; each controller has a controller processor and a controller to controller interface; CL20, L50-63; data can be transmitted from one array controller to another array controller). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Leshem, Espy, Horst et al.** and **Swanson et al.** with the system of **Brant et al.** that included at least one of the servers being operative to establish direct communication between the first and second controllers, and the first and second controllers being operative to maintain direct communication between the first and second controllers independent of the at least one CPU of the first server and the at least one CPU of the second server because that would allow data to be transmitted from one controller to another controller independent of the CPU, using the controller processor (CL20, L50-63; CL18, L42-52; Fig. 8; CL7, L20-28).

4.2 As per Claim 2, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** teach the system of claim 1. **Leshem, Espy, Horst et al., Hillis, Swanson et al.** and **Brant et al.** do not expressly teach that each storage device bypass circuit board includes a circuit which completes the connection of the CPU with the other storage device bypass circuits and their associated storage devices whether or not the storage device is present. **Dekoning et al.** teaches that each storage device bypass circuit board includes a circuit which completes the connection of the CPU with the other storage device bypass circuits and their associated storage devices whether or not the storage device is present (Fig 6; CL11, L30-60).

4.3 As per Claim 3, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** teach the system of claim 1. **Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** do not expressly teach each mass storage module including a module bypass circuit board. **Espy** teaches each mass storage module including a module bypass circuit board (Page 2, L5-23; Fig. 1, Item 40; Page 6, L7-16).

Leshem, Espy, Horst et al., Hillis, Dekoning et al. and **Brant et al.** do not expressly teach that each module bypass circuit board outputs electrical signals from the corresponding mass storage module via the optical input/output connector when light signals are received by the optical input/output connector. **Swanson et al.** teaches that each module bypass circuit board outputs electrical signals from the corresponding mass storage module via the optical input/output connector when light signals are received by the optical input/output connector (Fig. 2; CL1, L19-42).

4.4 As per Claim 5, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** teach the system of claim 1. **Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** does not expressly teach each of the first mass storage module and the second mass storage module including a module bypass circuit board. **Espy** teaches each of the first mass storage module and the second mass storage module including a module bypass circuit board (Page 2, L5-23; Fig. 1, Item 40; Page 6, L7-16).

Leshem, Espy, Horst et al., Hillis, Dekoning et al. and **Brant et al.** do not expressly teach that the module bypass circuit board of the first mass storage module outputs electrical signals from the first mass storage module to the second mass storage module via the optical input/output connector when light signals are received from the second mass storage module by the optical input/output connector. **Swanson et al.** teaches that the module bypass circuit board of the first mass storage module outputs electrical signals from the first mass storage module to the second mass storage module via the optical input/output connector when light signals are received from the second mass storage module by the optical input/output connector (Fig. 2; CL1, L19-42).

4.5 As per Claim 7, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** teach the system of claim 1. **Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** do not expressly teach that the storage devices (of each mass storage module) are disk drives. **Espy** teaches that the storage devices (of each mass storage module) are disk drives (Fig. 1, Items 12 of Items 10 and 110; Page 5, L16-17). One of ordinary skill in the art at the time of Applicants' invention would know the motivation to modify the

system of **Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** with the system of **Espy** that included the storage devices (of each mass storage module) being disk drives because the storage capacity of the mass storage module would be increased proportional to the number of plug-in disks for storing information. See **Hillis** (CL11, L29-33).

Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al. and **Brant et al.** do not expressly teach that the storage device bypass circuit boards are disk drive bypass circuit boards each having a connector to receive a disk drive. **Espy** teaches that the storage device bypass circuit boards are disk drive bypass circuit boards each having a connector to receive a disk drive (Fig. 1, Item 26 of Items 10 and 110; Page 5, L26-27; Page 5, L30 to Page 6, L2).

Per claim 10: **Leshem** teaches that the controller operates with a Fibre Channel protocol and the controller is Fibre Channel controller (CL2, L30-35; CL3, L33-36; CL3, L40-50).

4.6 As per Claim 11, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** teach the system of claim 1 **Leshem, Espy, Horst et al., Hillis, Swanson et al.** and **Brant et al.** do not expressly teach that the controller is an arbitrated dual channel Fibre Channel controller. **Dekoning et al.** teaches that the controller is an arbitrated dual channel Fibre Channel controller (CL1, L57-64; CL3, L56-64).

4.7 As per Claim 12, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** teach the system of claim 10. **Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** do not expressly teach that each storage device (of each mass

storage module) is a disk drive. **Espy** teaches that each storage device (of each mass storage module) is a disk drive (Fig. 1, Items 12 of Items 10 and 110; Page 5, L16-17).

Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al. and **Brant et al.** do not expressly teach that each storage device bypass circuit board comprises a disk drive bypass circuit board. **Espy** teaches that each storage device bypass circuit board comprises a disk drive bypass circuit board (Fig. 1, Item 26 of Items 10 and 110; Page 5, L26-27; Page 5, L30 to Page 6, L2).

Leshem, Espy, Horst et al., Hillis, Swanson et al. and **Brant et al.** do not expressly teach the disk drive bypass circuit board including a circuit which completes the connection of the CPU with the other drive bypass circuits and their associated disk drives whether or not the disk drive is present. **Dekoning et al.** teaches the disk drive bypass circuit board including a circuit which completes the connection of the CPU with the other drive bypass circuits and their associated disk drives whether or not the disk drive is present (Fig 6; CL11, L30-60).

4.8 As per Claim 13, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** teach the system of claim 12. **Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** do not expressly teach each mass storage module including a module bypass circuit board. **Espy** teaches each mass storage module including a module bypass circuit board (Page 2, L5-23; Fig. 1, Item 40; Page 6, L7-16).

Leshem, Espy, Horst et al., Hillis, Dekoning et al., and **Brant et al.** do not expressly teach that the module bypass circuit board outputs electrical signals from each mass storage module via the optical input/output connector when light signals are received by the optical

input/output connector. **Swanson et al.** teaches that the module bypass circuit board outputs electrical signals from each mass storage module via the optical input/output connector when light signals are received by the optical input/output connector (Fig. 2; CL1, L19-42).

5. Claims 6, 16, 19-21, 23, 24, 28-31 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Leshem** (U.S. Patent 5,729,763) in view of **Espy** (International Application WO 98/21660), and further in view of **Horst et al.** (U.S. Patent 6,496,940), **Hillis** (U.S. Patent 5,978,570), **Dekoning et al.** (U.S. Patent 6,055,228), **Swanson et al.** (U.S. Patent 6,580,531), **Brant et al.** (U.S. Patent 5,548,711) and **Harvey** (U.S. Patent 5,831,525).

5.1 As per Claim 6, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** teach the system of claim 1. **Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** do not expressly teach that each mass storage module includes a storage device bypass board connector for each of the storage device bypass circuit boards. **Espy** teaches that each mass storage module includes a storage device bypass board connector for each of the storage device bypass circuit boards (Fig. 1, Item 26 of Items 10 and 110; Page 5, L26-27; Page 5, L30 to Page 6, L2).

Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al. and **Brant et al.** do not expressly teach that each mass storage module includes a storage device bypass board connector for each of the storage device bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and storage devices for cooling purposes. **Harvey** teaches that each mass storage module

includes a storage device bypass board connector for each of the storage device bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and storage devices for cooling purposes (CL5, L14-50; Fig 1; Fig 2). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** with the system of **Harvey** that included each mass storage module including a storage device bypass board connector for each of the storage device bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and storage devices for cooling purposes because that would prevent overheating of the drive and the drive related computer hardware and loss of valuable data (CL2, L1-6).

5.2 As per Claim 16, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** teach the system of claim 11. **Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** do not expressly teach that the storage devices (of each mass storage module) are disk drives. **Espy** teaches that the storage devices (of each mass storage module) are disk drives (Fig. 1, Items 12 of Items 10 and 110; Page 5, L16-17).

Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al. and **Brant et al.** do not expressly teach that the storage device bypass circuit boards are disk drive bypass circuit boards. **Espy** teaches that the storage device bypass circuit boards are disk drive bypass circuit boards (Fig. 1, Item 26 of Items 10 and 110; Page 5, L26-27; Page 5, L30 to Page 6, L2).

Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al. and **Brant et al.** do not expressly teach that the at least one module includes a disk drive bypass board connector for each of the disk drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and disk drives for cooling purposes. **Harvey** teaches that the at least one module includes a disk drive bypass board connector for each of the disk drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and disk drives for cooling purposes (CL5, L14-50; Fig 1; Fig 2).

5.3 As per Claim 19, **Leshem** teaches a high speed mass storage system (CL1, L4-8; CL1, L33-37; Abstract, L11-14).

Leshem does not expressly teach a high speed mass storage system which is readily expandable to increase its storage capacity while the system is in operation; and first and second mass storage modules. **Espy** teaches a high speed mass storage system which is readily expandable to increase its storage capacity while the system is in operation (Page 1, L19-24); and first and second mass storage modules (Fig. 1, Items 10 and 110; Page 1, L19-24).

Leshem and **Espy** do not expressly teach a first server including a first controller and at least one CPU; and a second server including a second controller and at least one CPU. **Horst et al.** teaches a first server including a first controller and at least one CPU; and a second server including a second controller and at least one CPU (Fig. 1A, Items 12A and 14A; Items 12B and 14B; Abstract, L1-8).

Leshem and **Horst et al.** do not expressly teach each mass storage module including a plurality of plug-in storage devices for storing information. **Espy** teaches each mass storage module including a plurality of plug-in storage devices for storing information (Fig. 1, Items 12 of Items 10 and 110; Page 5, L16-17).

Leshem and **Horst et al.** do not expressly teach each mass storage module including a disk drive bypass circuit board associated with each disk drive. **Espy** teaches each mass storage module including a disk drive bypass circuit board associated with each disk drive (Fig. 1, Item 26 of Items 10 and 110; Page 5, L26-27; Page 5, L30 to Page 6, L2). One of ordinary skill in the art at the time of Applicants' invention would know the motivation to modify the system of **Leshem** and **Horst et al.** with the system of **Espy** that included each mass storage module including a disk drive bypass circuit board associated with each disk drive because that would enable connecting the storage device to the daisy-chain communication loop, when the device was enabled; and when failure or absence of a storage device was detected bypassing the storage device by connecting the daisy chain loop without the device See **Dekoning et al.** (CL11, L52-60).

Leshem and **Espy** do not expressly teach a disk drive bypass circuit board associated with each disk drive and including a disk drive connector at one edge thereof and a bypass board connector at another edge thereof, each disk drive being plugged into the disk drive connector on the disk drive bypass circuit board. **Harvey** teaches a disk drive bypass circuit board associated with each disk drive and including a disk drive connector at one edge thereof and a bypass board connector at another edge thereof, each disk drive being plugged into the disk drive connector on the disk drive bypass circuit board (CL5, L14-50; Fig 2, Items 226, 228 and 230).

Leshem, Horst et al. and **Harvey** do not expressly teach each mass storage module including a module bypass circuit board. **Espy** teaches each mass storage module including a module bypass circuit board (Page 2, L5-23; Fig. 1, Item 40; Page 6, L7-16).

Leshem, Espy, Horst et al. and **Harvey** do not expressly teach the module bypass circuit board including an optical input/ output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals. **Swanson et al.** teaches the module bypass circuit board including an optical input/ output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals (Fig. 2; CL1, L19-42).

Leshem, Horst et al., Swanson et al. and **Harvey** do not expressly teach that the optical input/output connectors of the first and second mass storage modules are connected by a fiber optic transmission medium such that signals are communicated between the first and second mass storage modules in the form of light. **Espy** teaches that the optical input/output connectors of the first and second mass storage modules are connected by a fiber optic transmission medium such that signals are communicated between the first and second mass storage modules in the form of light (Page 2, L29 to Page 3, L6; Page 6, L7-16.

In addition, **Hillis** teaches that the optical input/output connectors of the first and second mass storage modules are connected by a fiber optic transmission medium such that signals are communicated between the first and second mass storage modules in the form of light (Fig. 5; Fig. 6; CL10, L59 to CL11, L5; CL11, L29-33; CL11, L34-51).

Leshem teaches the first controller connecting the at least one CPU of the first controller with some of the disk drives through its associated drive bypass circuit board (CL3, L33-36;

CL3, L40-50). **Leshem, Espy, Swanson et al.** and **Hillis** do not expressly teach the first controller connecting the at least one CPU of the first controller with each disk drive; and the second controller connecting the at least one CPU of the second controller with each disk drive. **Horst et al.** teaches the first controller connecting the at least one CPU of the first controller with each disk drive; and the second controller connecting the at least one CPU of the second controller with each disk drive (CL16, L6-15; Fig. 1, Items 14A and 14B).

Leshem teaches the controller connecting the at least one CPU of the first controller with some of the disk drives through its associated drive bypass circuit board (CL3, L33-36; CL3, L40-50). **Leshem, Horst et al., Swanson et al.** and **Hillis** do not expressly teach the controller connecting the at least one CPU of the first controller with each of the disk drives through its associated drive bypass circuit board. **Espy** teaches the controller connecting the at least one CPU of the first controller with each of the disk drives through its associated drive bypass circuit board (Fig. 1, Item 16; Items 12, 22 and 26).

Leshem, Horst et al., Swanson et al. and **Hillis** do not expressly teach the first controller connecting the at least one CPU of the first controller with each disk drive through its associated drive bypass circuit board and through the module bypass circuit board such that a loop is formed between the output and input of the controller with each disk drive bypass circuit board and the module bypass circuit board in said loop. **Espy** teaches the first controller connecting the at least one CPU of the first controller with each disk drive through its associated drive bypass circuit board and through the module bypass circuit board such that a loop is formed between the output and input of the controller with each disk drive bypass circuit board and the module bypass circuit board in said loop (Page 2, L5-23; Fig 1, Item 40; Page 6, L7-16).

Leshem, Espy , Horst et al., Swanson et al. and **Hillis** does not expressly teach completing the loop whether or not a disk drive is plugged into the disk drive connector. **Dekoning et al.** teaches completing the loop whether or not a disk drive is plugged into the disk drive connector (Fig 6; CL11, L30-60).

Leshem, Espy , Horst et al., Swanson et al., Hillis and **Dekoning et al.** do not expressly teach at least one of the first and second servers being operative to establish direct communication between the first and second controllers, and the first and second controllers being operative to maintain direct communication between the first and second controllers independent of the at least one CPU of the first server and the at least one CPU of the second server. **Brant et al.** teaches at least one of the first and second servers being operative to establish direct communication between the first and second controllers, and the first and second controllers being operative to maintain direct communication between the first and second controllers independent of the at least one CPU of the first server and the at least one CPU of the second server (CL7, L20-28; each controller includes a separately programmable processor which can act independently of the CPU to control storage units; Fig. 4; there are two controllers connected to the CPU; each controller has direct communication with the other controller; CL12, L64 to CL13, L8; Fig. 8; each controller communicates with the other controller using the controller processor and data link interface, independent of the CPU; CL18, L42-52; each controller has a controller processor and a controller to controller interface; CL20, L50-63; data can be transmitted from one array controller to another array controller). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Leshem** with the system of **Brant et al.** that included at least one of the first and

second servers being operative to establish direct communication between the first and second controllers, and the first and second controllers being operative to maintain direct communication between the first and second controllers independent of the at least one CPU of the first server and the at least one CPU of the second server because that would allow data to be transmitted from one controller to another controller independent of the CPU, using the controller processor (CL20, L50-63; CL18, L42-52; Fig. 8; CL7, L20-28).

5.4 As per Claim 20, **Leshem, Espy, Horst et al., Hillis, Dekoning et al, Swanson et al., Brant et al.** and **Harvey** teach the system of claim 19. **Leshem, Horst et al., Hillis, Dekoning et al, Swanson et al., Brant et al.** and **Harvey** do not expressly teach that the module bypass circuit board of the first mass storage module completes the loop through the second module. **Espy** teaches that the module bypass circuit board of the first mass storage module completes the loop through the second module (Fig. 1, Items 40, 50, 52 of Item 110 and Item 10).

5.5 As per Claim 21, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al., Brant et al.** and **Harvey** teach the system of claim 19. **Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al., Brant et al.** and **Harvey** do not expressly teach each mass storage module including a module bypass circuit board. **Espy** teaches each mass storage module including a module bypass circuit board (Page 2, L5-23; Fig. 1, Item 40; Page 6, L7-16).

Leshem, Espy, Horst et al., Hillis, Dekoning et al., Brant et al. and **Harvey** do not expressly teach that the module bypass circuit board outputs electrical signals from each mass storage module via the optical input/output connector when light signals are received by the

optical input/output connector. **Swanson et al.** teaches that the module bypass circuit board outputs electrical signals from each mass storage module via the optical input/output connector when light signals are received by the optical input/output connector (Fig. 2; CL1, L19-42).

5.6 As per Claim 23, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al., Brant et al.** and **Harvey** teach the system of claim 19. **Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al., Brant et al.** and **Harvey** do not expressly teach each of the first mass storage module and the second mass storage module including a module bypass circuit board. **Espy** teaches each of the first mass storage module and the second mass storage module including a module bypass circuit board (Page 2, L5-23; Fig. 1, Item 40; Page 6, L7-16).

Leshem, Espy, Horst et al., Hillis, Dekoning et al., Brant et al. and **Harvey** do not expressly teach that the module bypass circuit board of each mass storage module outputs electrical signals from the first mass storage module to the second mass storage module via the optical input/output connector when light signals are received from the second mass storage module by the optical input/output connector. **Swanson et al.** teaches that the module bypass circuit board of each mass storage module outputs electrical signals from the first mass storage module to the second mass storage module via the optical input/output connector when light signals are received from the second mass storage module by the optical input/output connector (Fig. 2; CL1, L19-42).

5.7 As per Claim 24, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al., Brant et al.** and **Harvey** teach the system of claim 19. **Leshem, Horst et al., Hillis, Dekoning**

et al., Swanson et al., Brant et al. and **Harvey** do not expressly teach that each mass storage module includes a drive bypass board connector for each drive bypass circuit boards. **Espy** teaches that each mass storage module includes a drive bypass board connector for each drive bypass circuit boards (Fig. 1, Item 26 of Items 10 and 110; Page 5, L26-27; Page 5, L30 to Page 6, L2).

Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al., and **Brant et al.** do not expressly teach that each mass storage module includes a drive bypass board connector for each of the drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and disk drives for cooling purposes. **Harvey** teaches that each mass storage module includes a drive bypass board connector for each of the drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and disk drives for cooling purposes (CL5, L14-50; Fig 1; Fig 2).

Per claim 28: **Leshem** teaches that the controller operates with a Fiber Channel protocol and the controller is Fiber Channel controller (CL2, L30-35; CL3, L33-36; CL3, L40-50).

5.8 As per Claim 29, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al., Brant et al.** and **Harvey** teach the system of claim 19. **Leshem, Espy, Horst et al., Hillis, Swanson et al., Brant et al.** and **Harvey** do not expressly teach that the controller is an arbitrated dual channel Fiber Channel controller. **Dekoning et al.** teaches that the controller is an arbitrated dual channel Fiber Channel controller (CL1, L57-64; CL3, L56-64).

5.9 As per Claim 30, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al., Brant et al.** and **Harvey** teach the system of claim 29. **Leshem, Espy, Horst et al., Hillis, Swanson et al., Brant et al.** and **Harvey** do not expressly teach that each drive bypass circuit board includes a circuit which completes the connection of the CPU with the other storage device bypass circuits and their associated storage devices whether or not the storage device is present. **Dekoning et al.** teaches that each drive bypass circuit board includes a circuit which completes the connection of the CPU with the other storage device bypass circuits and their associated storage devices whether or not the storage device is present (Fig 6; CL11, L30-60).

5.10 As per Claim 31, it is a system claim having the same limitations as Claim 21. Therefore, Claim 31 is rejected based on the same reasoning as Claim 21, supra.

5.11 As per Claim 34, it is a system claim having the same limitations as Claim 24. Therefore, Claim 34 is rejected based on the same reasoning as Claim 24, supra.

6. Claims 8, 9, 17, 18, 25-27, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Leshem** (U.S. Patent 5,729,763) in view of **Espy** (International Application WO 98/21660), and further in view of **Horst et al.** (U.S. Patent 6,496,940), **Hillis** (U.S. Patent 5,978,570), **Dekoning et al.** (U.S. Patent 6,055,228), **Swanson et al.** (U.S. Patent 6,580,531), **Brant et al.** (U.S. Patent 5,548,711), **Harvey** (U.S. Patent 5,831,525) and **Kimura et al.** (U.S. Patent 5,414,591).

6.1 As per Claim 8, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** teach the system of claim 7. **Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al.** and **Brant et al.** does not expressly teach that each mass storage module includes a disk drive bypass circuit board connector for each of the drive bypass circuit boards. **Espy** teaches that each mass storage module includes a disk drive bypass circuit board connector for each of the drive bypass circuit boards (Fig. 1, Item 26 of Items 10 and 110; Page 5, L26-27; Page 5, L30 to Page 6, L2).

Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al. and **Brant et al.** do not expressly teach that each mass storage module includes a disk drive bypass circuit board connector for each of the drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors. **Harvey** teaches that each mass storage module includes a disk drive bypass circuit board connector for each of the drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors (CL5, L14-50; Fig 1; Fig 2).

Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al. and **Brant et al.** do not expressly teach that each drive bypass circuit board is a relatively flat circuit board with a connector on opposite edges, wherein one of the connectors is the connector which receives the disk drive and the other connector connects to the drive bypass circuit board connector. **Harvey** teaches that each drive bypass circuit board is a circuit board with a connector on opposite edges, wherein one of the connectors is the connector which receives the disk drive and the other

connector connects to the drive bypass circuit board connector (CL5, L14-50; Fig 2, Items 226, 228 and 230).

Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al., Brant et al. and **Harvey** do not expressly teach that each drive bypass circuit board is a relatively flat circuit board. **Kimura et al.** teaches that each drive bypass circuit board is a relatively flat circuit board (Fig 19; Fig 20; CL11, L19-52). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al., Brant et al.** and **Harvey** with the system of **Kimura et al.** that included each drive bypass circuit board being a relatively flat circuit board because that would allow the cooling air that has cooled the disk drive to flow over the circuit board, the board being along the cooling air flow (CL11, L34-38).

Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al., Brant et al. and **Kimura et al.** do not expressly teach the connectors, bypass circuit boards and drives being arranged such that when they are connected there is a path for air flow from outside the module alongside each bypass circuit board and its associated disk drive for cooling purposes without any backplane obstruction. **Harvey** teaches the connectors, bypass circuit boards and drives being arranged such that when they are connected there is a path for air flow from outside the module alongside each bypass circuit board and its associated disk drive for cooling purposes without any backplane obstruction (CL5, L14-20; Fig 1; Fig 2.

6.2 As per Claim 9, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al. Brant et al., Harvey** and **Kimura et al.** teach the system of claim 8. **Leshem, Horst et al.,**

Hillis, Dekoning et al., Swanson et al. Brant et al., Harvey and **Kimura et al.** do not expressly teach that each mass storage module is housed in an enclosure and at least one fan is mounted to force air from outside the enclosure through the spaces between the bypass boards and drives. **Espy** teaches that each mass storage module is housed in an enclosure and at least one fan is mounted to force air from outside the enclosure through the spaces between the bypass boards and drives (Page 5, L16-19).

6.3 As per Claims 17-18, these are system claims having the same limitations as Claims 8-9. Therefore, Claims 17-18 are rejected based on the same reasoning as Claims 8-9, supra.

6.4 As per Claim 25, **Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al. Brant et al.** and **Harvey** teach the system of claim 19. **Leshem, Horst et al., Hillis, Dekoning et al., Swanson et al. Brant et al.** and **Harvey** do not expressly teach that each mass storage module includes a drive bypass board connector for each drive bypass circuit boards. **Espy** teaches that each mass storage module includes a drive bypass board connector for each drive bypass circuit boards (Fig. 1, Item 26 of Items 10 and 110; Page 5, L26-27; Page 5, L30 to Page 6, L2).

Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al. and **Brant et al.** do not expressly teach that each drive bypass circuit board is a relatively flat circuit board with a connector on opposite edges, wherein one of the connectors is the connector which receives the disk drive and the other connector connects to the drive bypass circuit board connector. **Harvey** teaches that each drive bypass circuit board is a circuit board with a connector on opposite edges,

wherein one of the connectors is the connector which receives the disk drive and the other connector connects to the drive bypass circuit board connector (CL5, L14-50; Fig 2, Items 226, 228 and 230.

Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al., Brant et al. and **Harvey** do not expressly teach that each drive bypass circuit board is a relatively flat circuit board. **Kimura et al.** teaches that each drive bypass circuit board is a relatively flat circuit board (Fig 19; Fig 20; CL11, L19-52).

Leshem, Espy, Horst et al., Hillis, Dekoning et al., Swanson et al., Brant et al. and **Kimura et al.** do not expressly teach the connectors, bypass circuit boards and drives being arranged such that when they are connected there is a path for air flow from outside each mass storage module alongside each bypass circuit board and its associated disk drive for cooling purposes without any backplane obstruction. **Harvey** teaches the connectors, bypass circuit boards and drives being arranged such that when they are connected there is a path for air flow from outside each mass storage module alongside each bypass circuit board and its associated disk drive for cooling purposes without any backplane obstruction (CL5, L14-20; Fig 1; Fig 2).

6.5 As per Claim 26, it is a system claim having the same limitations as Claim 9. Therefore, Claim 26 is rejected based on the same reasoning as Claim 9, supra.

6.6 As per Claim 27, **Leshem** teaches that each drive bypass circuit board connector is mounted in the same plane in spaced relationship with each other (Fig 2A).

6.7 As per Claims 35-36, these are system claims having the same limitations as Claims 25-26. Therefore, Claims 35-36 are rejected based on the same reasoning as Claims 25-26, supra.

Conclusion

Response to Arguments

7.1 As per the applicants' argument that "the Examiner asserted that Brant et al. teaches at least one of the servers being operative to establish direct communication between the first and second controllers, and the first and second controllers being operative to maintain direct communication between the first and second controllers independent of the at least one CPU of the first server and the at least one CPU of the second server; the Examiner argued that it would have been obvious to one of ordinary skill in the art to modify the system of Leshem with the system of Brant et al., and that an artisan would have been motivated, because that would allow data to be transmitted from one controller to another controller independent of the CPU, using the controller processor; according to MPEP 706.02(j) the prior art reference (or references when combined) must teach or suggest all the claim limitations; the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure; the prior art references when combined do not teach or suggest all the claim limitations", the examiner respectfully disagrees.

Brant et al. teaches that the array controller includes a separately programmable processor which can act independently of the CPU to control (that means to communicate with)

the storage units (CL7, L254-28). The controllers have a controller processor, a controller-to-controller interface (which allows controller to controller direct communication independent of the CPU as shown in Fig. 8) and a controller-controller data link (for communicating information between the controllers) (CL18, L42-52). The data can be transmitted from one array controller over controller-controller data link to another array controller; the controller-controller interface is responsible for transmitting data to and from the array controller (CL20, L51-57). Therefore, the Examiner takes the position that according to MPEP 706.02(j) the prior art references teach all the claim limitations; the teaching or suggestion to make the claimed combination and the reasonable expectation of success are both found in the prior art.

7.2 As per the applicants' argument that "Brant et al., at column 7, lines 20-28, relating to the first embodiment shown in Fig. 1, teaches a CPU 1 coupled to a single array controller 3; Brant et al., in Fig. 4 and column 12, line 64 to column 13, line 8, relating to the third embodiment, discloses a CPU 1 coupled to first and second array controllers 403 and 405; in Fig. 8 and at column 18, lines 42-52, and column 20, lines 50-63, relating to the fifth embodiment, Brant et al. discloses a CPU 1 coupled to first and second array controllers 801, 802; it is thus clear that in Brant et al., there is no disclosure of first and second servers each including a controller and at least one CPU, wherein at least one of the servers is operative to establish direct communication between the controllers of the first and second servers, and the controllers being operative to maintain direct communication between them independent of the CPU's of the first and second servers", the Examiner respectfully disagrees.

Though a CPU is connected to the array controller in Fig.1, Fig. 4 and Fig. 8., Brant et al. clearly states that the array controllers have the capability to communicate with the storage devices independently of the CPU since they have a controller processor which can perform the function of the CPU. Brant et al. also states that the controllers communicate independently of the CPU through the controller-to-controller interface. See Paragraph 7.1 above.

7.3 As per the applicants' argument that "none of the references cited teach, disclose or suggest, either individually or in combination, first and second servers each with at least one CPU, and at least one of the first and second servers being operative to establish direct communication between their respective first and second controllers, and said first and second controllers being operative to maintain direct communication between the first and second controllers independent of the at least one CPU of the first server and the at least one CPU of said second server", the Examiner directs Applicant's attention to Paragraph 4.1 and 7.1 above

7.4 As per the applicants' argument that "Harvey does not teach, disclose or suggest first and second servers each with at least one CPU, and at least one of the first and second servers being operative to establish direct communication between their respective first and second controllers, and said first and second controllers being operative to maintain direct communication between the first and second controllers independent of the at least one CPU of the first server and the at least one CPU of said second server", the Examiner directs Applicant's attention to Paragraph 4.1 and 7.1 above

7.5 As per the applicants' argument that "Kimura et al. also does not teach, disclose or suggest first and second servers each with at least one CPU, and at least one of the first and second servers being operative to establish direct communication between their respective first and second controllers, and said first and second controllers being operative to maintain direct communication between the first and second controllers independent of the at least one CPU of the first server and the at least one CPU of said second server", the Examiner directs Applicant's attention to Paragraph 4.1 and 7.1 above

ACTION IS FINAL

8. Applicant's arguments with respect to claim rejections under 35 USC § 103 (a) are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
May 5, 2006